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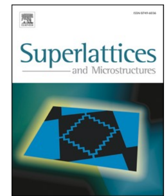

Reliability concern of quasi-vertical GaN Schottky barrier diode under high temperature reverse bias stress

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ABSTRACT

In this paper, the reliability of quasi-vertical GaN Schottky barrier diodes under high temperature reverse bias (HTRB) stress has been investigated. The test results indicate that the stress applied on the devices makes reverse leakage current decrease, but the forward performance, capacitance and reverse recovery performance show negligible changes. With the help of experiments and T-CAD simulations, it is demonstrated that there is trapping process of hot electrons along vertical sidewall of the device under high reverse voltage stress, which leads to the decrease of reverse leakage current. An empirical model can be used to predict the variations and good coincidences can be observed based on the acquired experiment data. Moreover, long time over voltage stress on the device leads to the direct failure. By using the infrared thermography analysis and T-CAD simulations, the failure mechanism has been also illustrated.

1. Introduction

GaN-based devices are considered as the candidates for the future power applications due to the excellent physical properties of GaN material [1,2]. Vertical structure diodes have attracted great attentions since they have higher breakdown voltage (BV) and current capability per unit wafer area compared with lateral structure diodes [3,4,5]. However, there are challenges to manufacturing fully-vertical GaN diodes upon cheap substrates [6]. By GaN deep etching process, it is relatively simple to make the mesa isolation and access the cathode region [7]. In this way, quasi-vertical structure diodes can be acquired, which can avoid the limitations of the substrate and are easy to be commercialized, while the high performances can be also maintained.

Despite the excellent performances of quasi-vertical GaN diodes, it is inevitable to investigate the reliabilities of quasi-vertical GaN diodes when applying them on power electronic systems. Nowadays, the GaN diodes in power electronic systems are working under high reverse voltage (V_R) bias and high ambient temperature. Thereby, the studies on the reliability of the quasi-vertical GaN diodes under high V_R and high temperature stress are highly required. Among the previous studies on quasi-vertical diodes, most of them are focused on the manufacturing process and performance improvements, few articles about reliabilities of such devices can be referred [8,9,10]. In this paper, high temperature reverse bias (HTRB) stress tests on the GaN-based quasi-vertical Schottky barrier diodes (SBDs) are carried out, and the physical mechanisms behind the electrical behaviours are discussed with the help of experiments and

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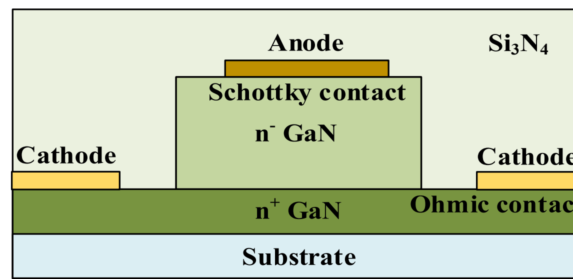

Fig. 1. Schematic cross section of the experimented quasi-vertical GaN SBD device.

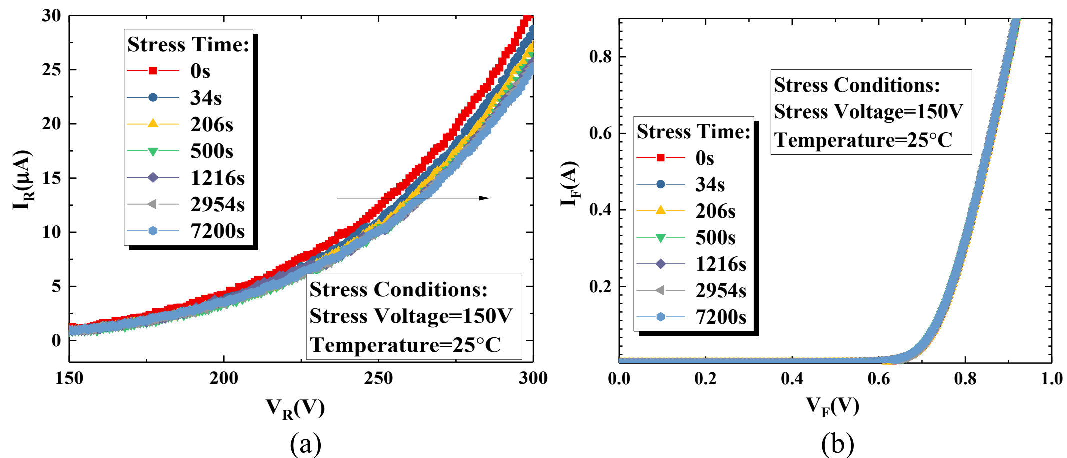

Fig. 2. Measured static electrical performances after 150 V V_R stress at room temperature. (a) I_R variations under different stress time. (b) Forward current (I_F) variations under different stress time.

Silvaco Atlas technology computer-aided design (T-CAD) simulations.

2. Device structure and experiments

Fig. 1 shows the schematic cross section of the experimented quasi-vertical GaN SBD device. The GaN layers were grown on a 100 mm sapphire substrate by metalorganic chemical vapor deposition (MOCVD). A Si-doped ($\sim 5 \times 10^{19}$) n + GaN layer was grown firstly, followed by the 6 μm n- ($\sim 1 \times 10^{16}$) GaN layer epitaxy. Then deep recesses were made by inductively coupled plasma (ICP) dry etching to access the cathode region. The first 5 nm Si_3N_4 passivation layer was deposited by MOCVD and the second Si_3N_4 passivation layer was deposited by plasma enhanced chemical vapor deposition (PECVD). The anode region and cathode region was opened to allow the formation of contacts by TiN and Ti-based metal stacks, respectively. The anode length, cathode length and GaN mesa width are 50 μm, 20 μm and 80 μm, respectively. The rated reverse breakdown voltage and forward operation current of the experimented diode are 300 V and 5 A, respectively.

To investigate the reliability of the quasi-vertical GaN SBD devices used in power electronic systems, HTRB stress tests are applied on the diodes. The devices under test are heated by ceramic heating sheet and monitored by thermal infrared imager. All the voltage stress procedures and static parameter measurements are accomplished by Agilent B1505A, the capacitances are measured by Agilent E4980A, and the reverse recovery characteristics are measured by the self-designed printed circuit board (PCB) [11]. Before each measurement, the high temperature stress is firstly removed and the devices are naturally cooled down to room temperature. Then, the parameter measurements are carried out immediately after the voltage stress is removed.

3. Measurements and discussions

3.1. Normal high reverse voltage stress

Fig. 2 shows the measured reverse and forward characteristics after 150 V V_R stress at room temperature. It can be seen that the reverse leakage current (I_R) decreases with stress time but the forward characteristic is unchanged. The dynamic performances including capacitance performance and the reverse recovery performance under the same stress condition are also measured, as shown in Fig. 3. The C-V characteristics are tested at 1 MHz frequency, and the reverse recovery current (I_{RR}) are tested at 50 V switching

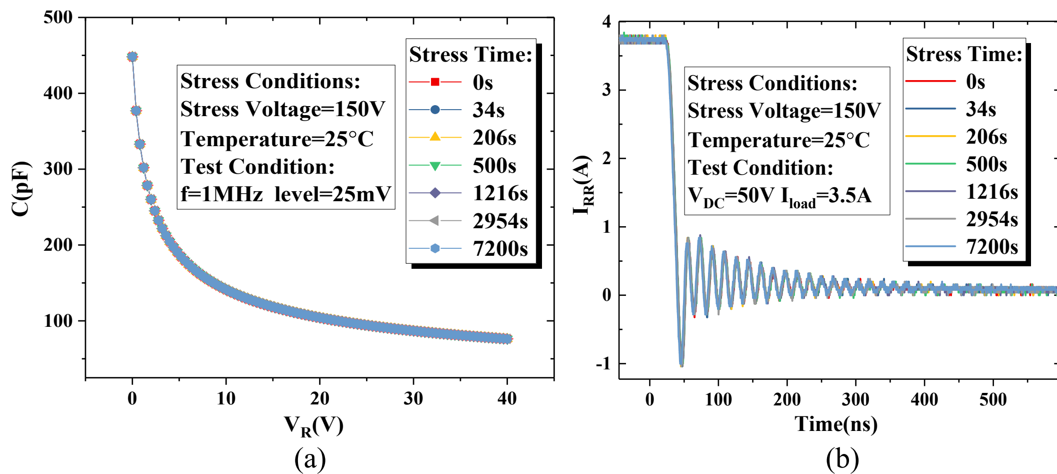

Fig. 3. Measured dynamic electrical performances after 150 V V_R stress at room temperature. (a) Capacitance variations under different stress time. (b) I_{RR} variations under different stress time.

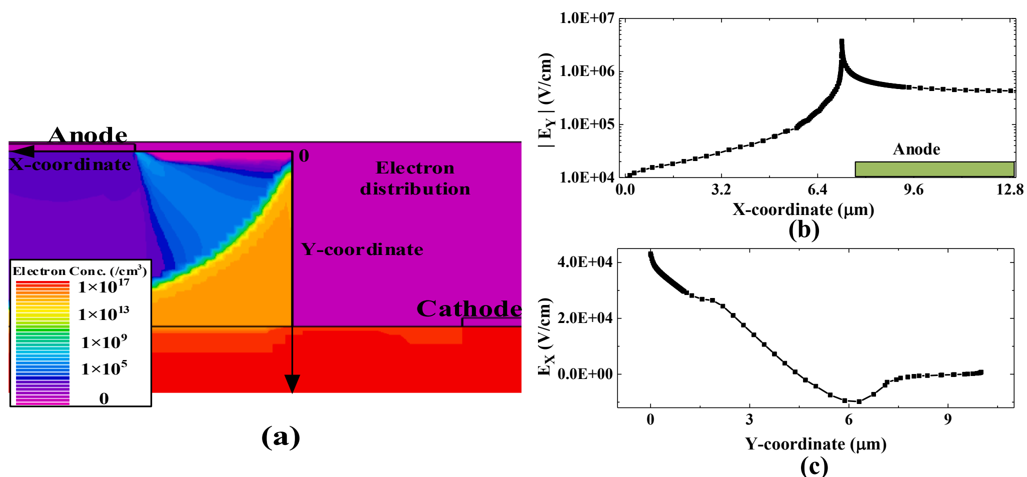

Fig. 4. Simulated electron distribution and extractions of electric field of the investigated device at $V_R = 150$ V. (a) Electron distribution and established coordinate system for electric field. (b) Extraction of electric field along lateral surface. (c) Extraction of electric field along sidewall.

voltage and 3.5 A load current. It can be seen that all the dynamic characteristics are also unchanged with stress time. The results above indicate that the high V_R stress only impacts the reverse characteristic. To understand the physical mechanisms of the phenomena, T-CAD simulations and further test procedures are carried out.

The simulated electron concentration distribution of the device at $V_R = 150$ V and 25 °C is shown in Fig. 4(a). It can be seen from the picture that the leakage current is formed at the corner of anode electrode. Unfortunately, there is possibility for current path to be influenced by the interface states along lateral surface and sidewall of GaN mesa, which result from the roughness of the material interface. The density of the interface states is related to many factors, such as the manufacturing facilities and the etching methods. Tough the ICP dry etching method is carried out, the roughness along sidewalls is still hard to be eliminated absolutely. In fact, not only the interface states along lateral surface, but also those along sidewall have influences on the electrical performances of the devices and even bring reliability problems [12,13]. Herein, it is reasonable to consider that carriers can be accumulated along the surface and interface of the quasi-vertical SBD under the high reverse voltage stress. If carriers are accumulated at anode meatal/GaN interface, the forward performances must be influenced, which are inconsistent with the experiment results. Thus, only the electrical performances of the diodes with accumulated carriers along lateral surface and vertical sidewall are investigated. Fig. 4(b) and (c) shows the extractions of electric field values along the lateral surface and vertical sidewall. To be noted, the coordinate system is also shown in Fig. 4(a). Fig. 4(b) shows the longitudinal electric field (E_Y) at lateral surface of the GaN mesa, which is negative value in the coordinate system, meaning that holes accelerated by electric field can move towards the lateral surface. Fig. 4(c) shows the transverse electric field (E_X) at vertical sidewall of the GaN mesa, which is positive value in the coordinate system, meaning that electrons accelerated by electric field can move towards the sidewall. Once the hot carriers from GaN layers get enough energy, it is easy for them to be accumulated at the surface or sidewall. As the results, the leakage current paths are impacted. To identify whether electrons or holes

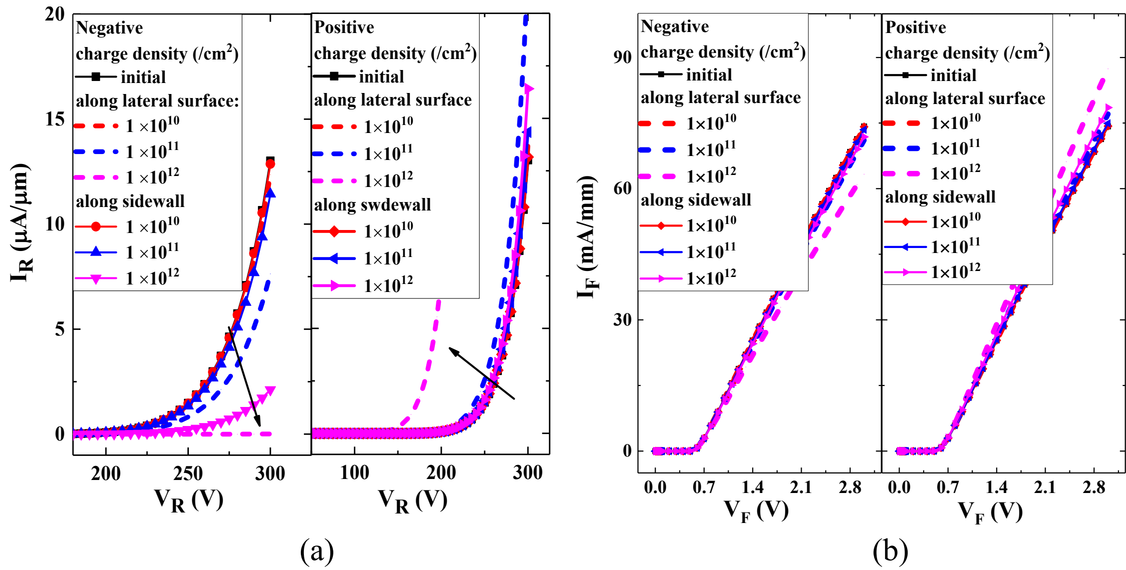

Fig. 5. Simulated static electrical performances with charges along surface. (a) I_R variations under different charge densities. (b) I_F variations under different charge densities.

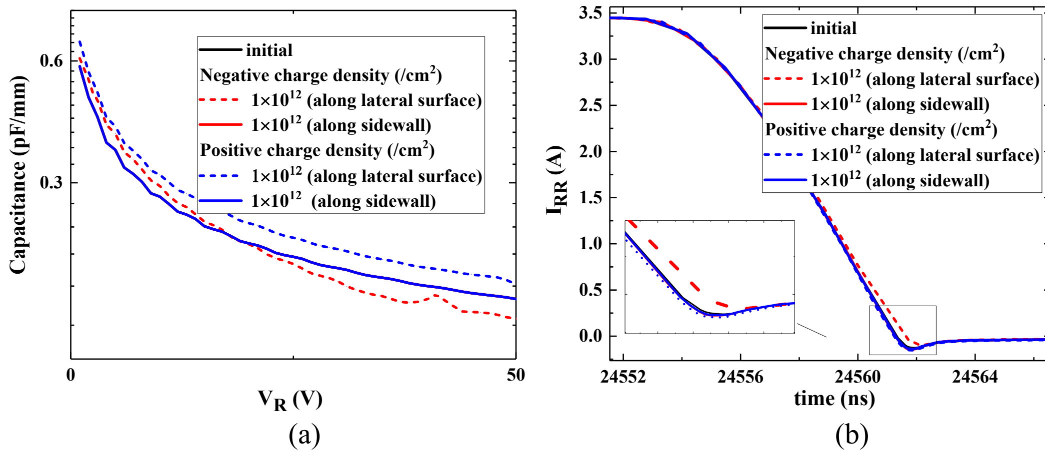

Fig. 6. Simulated dynamic electrical performances with charges along surface and sidewall. (a) Capacitance variations with charges at different positions. (b) I_{RR} variations with charges at different positions.

are accumulated, positive charges and negative charges are added to the lateral surface and vertical sidewall in the T-CAD simulations, respectively. The simulation results are presented in the following pictures.

Fig. 5 shows the simulated static electrical performances of the devices with charges of different properties and densities along lateral surface and vertical sidewall at 25 °C. From Fig. 5(a), negative charges along lateral surface can lead to more reduction in I_R than those along vertical sidewall with the same charge density. However, positive charges along lateral surface lead to more increase in I_R than those along sidewall. From Fig. 5(b), only charges along lateral surface can make the forward current change obviously, performed as I_F increased by positive charges and I_F decreased by negative charges. Moreover, dynamic electrical performances of the devices with charges along lateral surface and vertical sidewall are also investigated by simulations, as shown in Fig. 6. The frequency in the capacitance simulations is 1 MHz, the switching voltage in the reverse recovery simulations is 50 V and the load current is 3.5 A. It can be seen that charges along lateral surface have influences on capacitance characteristic and the reverse recovery characteristic but charges along sidewall do not. The physical mechanisms behind the phenomena above are analysed by the furthermore simulation results.

Fig. 7 shows the potential lines and electron concentration distribution of the simulated devices with charges at 25 °C. The density of both the positive and negative charges in the simulations is 1×10^{12} cm^{-2}. From the pictures, the charges along lateral surface and vertical sidewall can change the potential nearby, making the depletion region shrink or expand. In this way, the electrical performances are changed. The charges along lateral surface have relatively obvious influence on the distribution of carries under anode

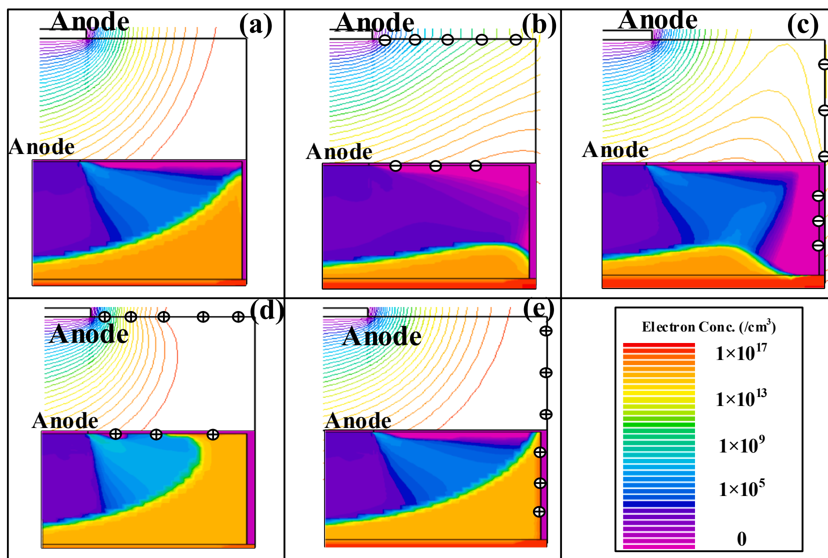

Fig. 7. Potential lines and electron concentration distribution of the devices with charge density of 1×10^{12} cm^{-2}. (a) Fresh device (b) Device with negative charges along lateral surface (c) Devices with negative charges along sidewall (d) Devices with positive charges along lateral surface (e) Devices with positive charges along sidewall.

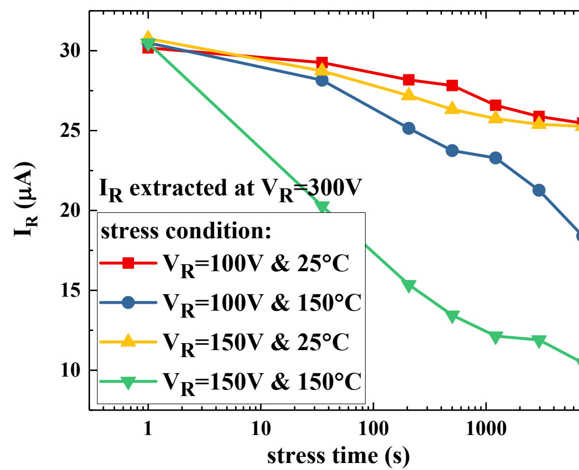

Fig. 8. Measured decrease tendency of I_R under different stress conditions.

electrode and lead to the variations of I_F, I_{RR} and capacitance, as shown in Fig. 6. However, the charges along vertical sidewall have little influence on the anode region but lead to the variations of I_R.

Considering the difficulties of the etching process, the material quality of the sidewall is worse than the lateral surface, it is reasonable that more carriers will get accumulated along vertical sidewall under the high V_R bias than along lateral surface. Taking the measurement results and simulation results into considerations, it can be concluded that hot electrons accelerated by the electrical field get accumulated along vertical sidewall during the high V_R stress, which leads to the expanding of depletion region in the n^- GaN layer, as a result, making the decrease in I_R without impacting other electrical performances. To verify the above point of view, further supporting tests are carried out.

Fig. 8 shows the decrease tendency of I_R under different stress conditions. 100 V V_R stress and 150 V V_R stress tests at room temperature and 150 °C are carried out, respectively. The I_R are tested at $V_R = 300$ V. Under higher temperature stress and higher V_R stress, I_R decreases more with time. To be noted, the forward performances and dynamic performances are also monitored, and all the measured parameters show negligible changes. It is true that higher electric field and higher temperature will induce more hot electrons [14], as a result, more electrons get accumulated along sidewall and I_R decreases more. The results in Fig. 8 prove that there is trapping process in the devices under HTRB stress.

An empirical model for electrical parameter degradations due to hot-carriers injection is used to predict the I_R shifts after HTRB stress. The model is described as [15]:

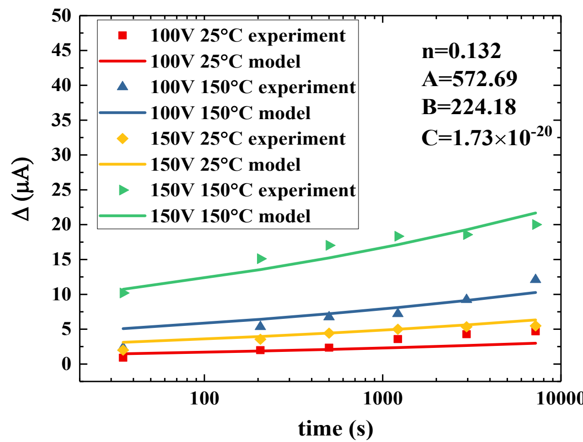

Fig. 9. The fitting results of the model for hot-carriers degradations based on experiment results.

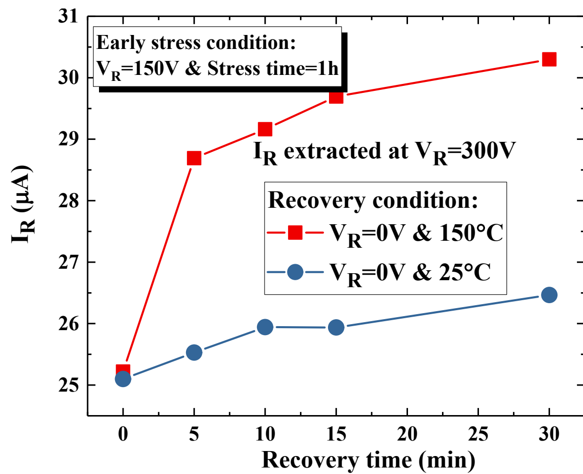

Fig. 10. Measured recovery tendency of I_R with time under different temperatures.

$$\Delta = At^n e^{-\left(\frac{B}{v}+\frac{C}{kT}\right)} \quad (1)$$

where n, A, B and C are constants, v (V) is the stress voltage, T (K) is the stress temperature, t (s) is the stress time, Δ (μA) is the shifts of I_R. The results shown in Fig. 9 are acquired by fitting the data in Fig. 8. It can be seen that the model is appropriate for predicting the parameter shifts of the investigated devices under HTRB stress.

The recovery tests have also been carried out. Fig. 10 presents the recovery tendency of I_R with time under different temperatures. The devices are stressed under $V_R = 150$ V at room temperature for 1 h, then, the recovery tests are carried out at room temperature and 150 °C respectively. From the picture, I_R is recovering with time under both the two temperature conditions. Fig. 10 also proves that there is de-trapping process in the devices during recovery tests, and higher temperature results in faster recovery process. Since the high voltage stress is removed, the electrons trapped by interface states along sidewall are gradually released with the time. However, the trapped electrons get small extra energy at room temperature and the release speed is slow, thus, the trapped electrons still expand the depletion region and make the shifts of measured I_R. At high temperature, the trapped electrons get extra energy and escape from the traps easily. In this way, the trapped electrons get released completely in a shorter time compared with the devices recovered at room temperature, performed as the I_R recovers faster. Consequently, with the help of experiments and T-CAD simulations, it is concluded that the decrease of I_R under high reverse bias and high temperature stress results from the trapping process of hot electrons at the sidewall.

3.2. *Over reverse voltage stress*

To evaluate the electrical behaviours of quasi-vertical GaN SBD under high V_R stress comprehensively, over reverse voltage stress tests are accomplished. By applying 250 V V_R stress to the device for a week at room temperature, the failure can be observed, as seen in

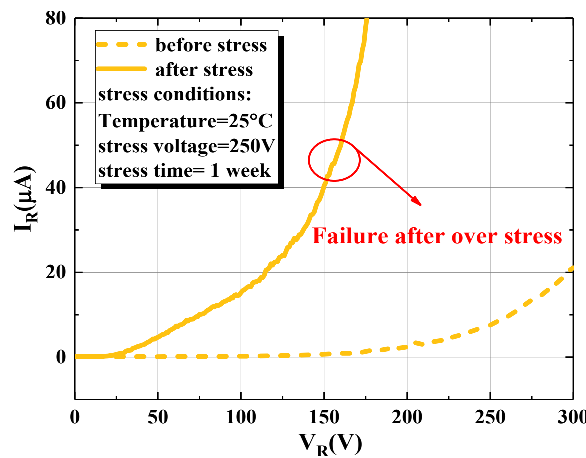

Fig. 11. Measured I_R variations under over voltage stress.

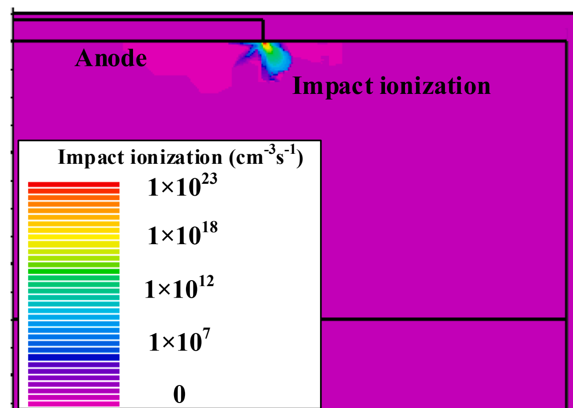

Fig. 12. Simulated impact ionization distribution of the investigated device at $V_R = 250$ V.

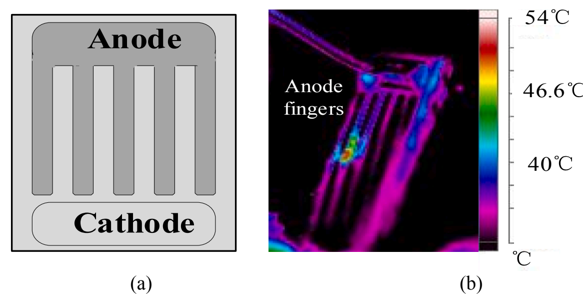

Fig. 13. Information of the experimental analysis on the destroyed device (a) schematic view of the device after decapping. (b) Infrared thermography of the failure die.

Fig. 11. To investigate the phenomenon, T-CAD simulations and the infrared thermography analysis are also carried out.

Fig. 12 shows the simulated impact ionization distribution of the quasi-vertical diode at $V_R = 250$ V. It can be seen that the impact ionization of the device occurs at the anode electrode corner. During the long time high V_R stress, the impact ionization can damage the device, which may lead to the failure. The schematic view of the failure device after decapping is shown in Fig. 13(a), the anode fingers correspond to anode metal on the GaN mesas. Before the infrared thermography analysis, a 10 mA constant current is applied from cathode to anode to heat the failure device. The infrared thermography shown in Fig. 13(b) indicates that the failure point is at the anode finger, where the impact ionization centre is. Taking the simulation and infrared thermography analysis results into consideration, it is concluded that the impact ionization at the anode corner results in the failure of the tested device.

4. Conclusion

The reliability of quasi-vertical GaN SBD under HTRB stress has been investigated in this paper. From the stress test results, the HTRB stress has no influence on the forward and dynamic performances. However, the reverse leakage current of the device decreases after HTRB stress. By simulations and further experiments, it is demonstrated that the hot electrons get trapped at the sidewall under the high V_R stress, resulting in the decrease of I_R once the stress is cancelled. Also, an empirical model for hot carriers induced degradations are used to predict the I_R shifts of the investigated device. Good coincidences can be observed between the experiment results and the model. Moreover, the failure of the device can be observed under over reverse voltage stress, this is because the device is damaged by the impact ionization at anode electrode corner.

Acknowledgments

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